**Computer Architecture (2)**

**Rubric - Project Final Submission**

Please fill in the 2nd column of the following table:

|  |  |
| --- | --- |
| Total number of Pipeline Stages | 6 |
| Correctness of the design checked (compared to a software implementation)? Yes/No | yes |
| Design is implemented in Verilog? Fully/Partially | Fully |
| Simulations show:  1-only partial results of stages  2- only final results  3- Both partial and final results | 3- Both partial and final results |
| Simulations show cycle by cycle results? Yes/No | Yes |
| Number of simulated clock cycles? | 24 |
| Design is compared (analytically) with single-cycle implementation?Yes/No | Yes |